Progressive Radiation Hardness Assurance for COTS SmallSat Avionics Beyond LEO

1st Jasper Dijks 2nd Jorge de Francisco
Aerospace Systems, Royal Netherlands Aerospace Centre (NLR), Amsterdam, Netherlands
{jasper.dijks, jorge.de.francisco}@nlr.nl

***Abstract*—As SmallSat missions extend beyond Low Earth Orbit (LEO), traditional Radiation Hardness Assurance (RHA) approaches based on linear qualification workflows are increasingly mismatched with Commercial-Off-The-Shelf (COTS)-based avionics programmes. This paper presents a progressive RHA methodology applied to photonic and electronic avionics that treats radiation assurance as an iterative design activity. The methodology is grounded in a fundamental asymmetry between the two domains. Photonic subsystems exhibit parametric degradation, while electronic subsystems are susceptible to stochastic failure modes. This asymmetry motivates a multi-pathway Hardware-in-the-Loop (HiL) fault injection platform built around a Zynq UltraScale+ Multi Processor System-on-Chip (MPSoC) modem for Optical Communication Terminal (OCT) applications. The platform combines a variety of fault injection methods, enabling independent and combined assessment of fault mechanisms across the full signal chain. The progressive approach shifts risk identification earlier in the design cycle, reducing reliance on costly late-stage qualification and enabling more efficient allocation of beam facility resources.**

***Index Terms*—Commercial-Off-The-Shelf (COTS), Field Programmable Gate Array (FPGA), Optical Communication Terminal (OCT), Radiation Hardness Assurance (RHA), SmallSat**

I. Introduction

THERE are increasing challenges for Radiation Hardness Assurance (RHA) of Commercial-Off-The-Shelf (COTS)-based avionics in mission trajectories extending beyond Low Earth Orbit (LEO). As SmallSat programmes target these, Size, Weight, Power and Cost (SWaP-C) constraints continue to drive adoption of COTS components [1]. Traditional RHA workflows with formal qualification standards are often incompatible with the resource constraints and development pace of SmallSat programmes targeting these environments for longer durations [2]. A systematic review of commercial space avionics identified a shift towards mission-tailored, system-level assurance that treats RHA as an iterative design activity rather than a final qualification gate [3].

Existing work addresses parts of this gap but not its full extent. Test-in-the-loop methods have been demonstrated for RISC-V dependability validation [4], [5], and system-level radiation testing under particle beams has been developed as a cost-effective alternative to component-level qualification [6], but neither approach offers controllable laboratory fault injection for heterogeneous photonic and electronic avionics. Individual fault injection techniques are mature in their respective domains, including model-implemented and emulation-based digital injection [7], [8], electrical transient injection for analogue signal chain characterisation [9], and pulsed laser testing for device-level Single Event Transient (SET) susceptibility [10]. None of these efforts integrates these methods into a single platform targeting avionics with photonic and electronic architectures, where cross-domain fault propagation is a dominant system-level risk [11], [12].

This work addresses these gaps through three contributions.

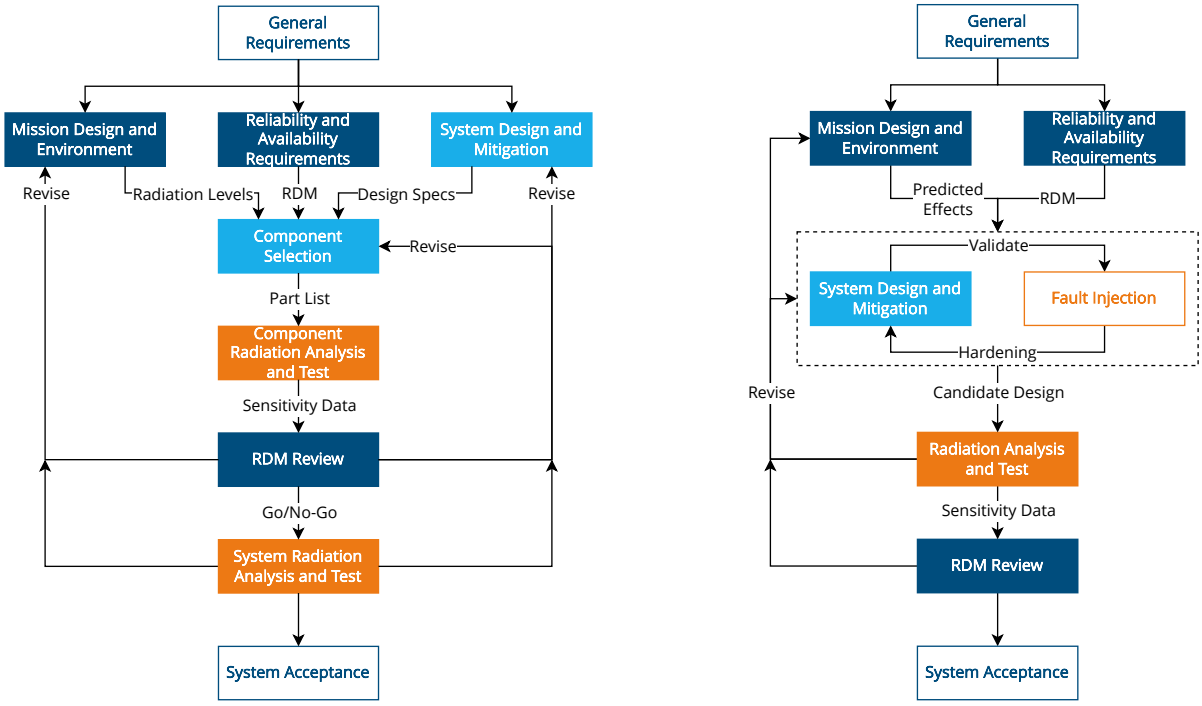
- A progressive, feedback-driven RHA methodology for COTS-based avionics, structured around two nested feedback loops.
- A multi-pathway Hardware-in-the-Loop (HiL) fault injection platform, currently under commissioning, integrating digital, electrical, optical and pulsed laser injection within a single laboratory environment, built around a Zynq UltraScale+ Multi Processor System-on-Chip (MPSoC) Field Programmable Gate Array (FPGA) modem for Optical Communication Terminal (OCT) applications.
- Synthesis of the asymmetry between photonic parametric degradation and electronic stochastic failure modes as the organising principle for the multi-pathway platform architecture.

This methodology is studied using photonic and electronic OCT avionics. Section II describes the progressive RHA methodology. Section III presents the multi-pathway HiL fault injection platform. Section IV discusses the implications and generalisability of the approach, and Section V concludes.

II. Progressive RHA Methodology

The progressive RHA approach is structured around two nested feedback loops operating at different timescales, as illustrated in Figure 1. Traditional RHA workflows allow iteration in principle, but each cycle requires a radiation test campaign, limiting practical iteration to one or two passes before the design is committed [3]. The progressive approach introduces a fast inner loop between system design and laboratory fault injection, enabling many iterations on architecture and mitigation choices with reduced beam facility access. A slower outer loop validates the resulting design against radiation testing, with test outcomes feeding back into both the design and the predicted effects that guide subsequent iterations. This aligns with the rapid learning cycle methodology [3] for COTS-based space systems and with the

This work received funding from the Dutch National Growth Fund through the NXTGEN HIGHTECH programme.



(a) Traditional RHA process [3].

(b) Proposed progressive RHA method.

Fig. 1: Comparison of RHA processes. The progressive method nests a fast inner loop between system design and laboratory fault injection inside a slower outer loop in which radiation testing validates the design and refines the predicted effects driving the next iteration.

test-in-the-loop methods [4], [5]. The progressive approach does not replace established frameworks from major space agencies, but it tailors the execution order and gating logic for COTS-based programmes where the architecture is still open to revision and beam access is restricted, requiring earlier risk identification. The methodology suits programmes willing to adopt risk management approaches that differ from traditional flight qualification, accepting higher residual risk in exchange for faster iteration and earlier vulnerability discovery. The methodology adapts this iterative paradigm to photonic and electronic avionics and operates across three main stages.

A. Radiation Effect Prediction

The first stage produces a predicted set of radiation effects and failure mechanisms for the target mission, against which subsequent screening and testing are evaluated. The external radiation environment is first characterised using environmental models such as SPENVIS [13], establishing Total Ionizing Dose (TID), Displacement Damage Dose (DDD) and Single Event Effect (SEE) rate requirements for the target mission. Where required, radiation transport codes such as GEANT4 [14] translate this external environment into device-level charge deposition and particle interaction profiles, providing the physical basis for the fault scenarios used in laboratory injection. The resulting predictions identify the dominant failure mechanisms expected per subsystem and directly inform the selection of test modalities and Device Under Tests (DUTs) for subsequent screening. They also provide the reference set against which radiation test outcomes are compared in the outer feedback loop.

B. Iterative Design and Fault Injection

The fast inner loop of the methodology iterates through system design, mitigation choices, and laboratory fault injection on a HiL platform, described in detail in Section III. The fault injection model is initialised from the radiation effect predictions of Section II-A and refined as those predictions improve through radiation testing in the outer loop. Many design-injection iterations can be completed before the candidate design is submitted to radiation validation, enabling mitigation effectiveness and system-level resilience to be evaluated without beam facility access.

C. Design Validation under Radiation

The candidate design produced by the inner loop is validated under radiation conditions representative of the target mission. Test modalities, beam parameters and DUTs are selected based on the predicted radiation effects and dominant failure mechanisms identified in the prediction stage and refined through

laboratory fault injection, focusing beam facility resources on the specific devices, mechanisms and conditions where uncertainty and risk remain highest. Validation has two purposes. The first is to confirm that the candidate design survives the radiation conditions of the target mission. The second is to validate the radiation effect predictions established in the first stage, with deviations between predicted and observed effects feeding back into both the laboratory injection campaigns and the prediction model that guides subsequent design iterations.

This staged structure defers costly validation campaigns until sufficient evidence exists to focus them effectively, prioritising learning over standardisation. The increased iteration rate enabled by laboratory fault injection accelerates the learning cycle, helping designers understand not only that a COTS-based system is reliable, but why it is reliable. This understanding is the prerequisite for managing the growing complexity of COTS architectures in space missions.

III. Hardware-in-the-Loop Platform

The methodology described in Section II requires a fault injection capability that addresses two distinct domains. Studies of photonic and electronic OCT avionics have established that electronic subsystems are dominated by memory-origin fault propagation in the digital processing chain, while photonic detector subsystems are dominated by sensitivity degradation and a power-independent Bit Error Rate (BER) floor in the receiver chain [3], [15], [16]. No single injection technique addresses both, and beam facility access is inherently limited and costly, making iterative design-test-redesign cycles impractical. The HiL platform therefore adopts a multi-pathway architecture, summarised in Table I, combining digital, electrical and optical fault injection within a single laboratory environment, enabling independent and combined assessment of degradation types across the full signal chain.

TABLE I
MAPPING OF RADIATION RESPONSE CHARACTERISTICS TO FAULT INJECTION PATHWAYS FOR THE OCT MODEM PLATFORM.

	Electronic	**Photonic**
Degradation type	Stochastic	Parametric
Dominant mechanism	Memory-origin faults	Sensitivity shift, BER floor
Mitigation techniques	ECC, Scrubbing	Link budget margin, FEC
Injection pathways	Digital, Electrical, Pulsed laser	Optical, Pulsed laser
Key observable	SDC rate, SEFI rate	BER, AGC recovery

A. Platform Architecture

The fault injection platform, illustrated in Figure 2, is built around an AMD Zynq UltraScale+ MPSoC (ZCU106 evaluation board) running a representative optical communication modem pipeline. The FPGA fabric implements a Pseudo-Random Binary Sequence (PRBS) signal generator and BER checker, providing a controlled data stream for link-level characterisation. The processing system side of the Zynq handles modem control logic, monitoring and communication with the host workstation.

The optical bench includes a transmitter path with a Mach-Zehnder Modulator (MZM) for signal modulation, a fibre-coupled receiver with photodetector, and monitoring equipment for optical power measurements. Together, the FPGA modem and optical bench form a closed-loop optical communication link operating under flight-representative conditions. The architecture provides four complementary fault injection pathways:

- a digital pathway targeting the FPGA processing fabric (Section III-B);
- an electrical pathway targeting component I/O interfaces on the Printed Circuit Board (PCB) (Section III-C);
- an optical pathway injecting noise into the fibre-coupled receiver path (Section III-D);
- a pulsed laser pathway targeting the detector and FPGA (Section III-E).

B. Digital Fault Injection via Simulink/HDL Coder

The ZCU106 is interfaced with MATLAB through the Simulink/HDL Coder toolchain, enabling direct interaction with the FPGA processing fabric during operation. Model-implemented fault injection, originally developed for safety-critical cyber-physical systems [7], can be adapted for FPGA-based space avionics by combining it with emulation-based Single Event Upset (SEU) injection techniques [8] and the Simulink/HDL Coder toolkit for a fast prototyping methodology [17]. The HDL Coder interface provides read and write access to registers, memory blocks and configuration state within the deployed design through JTAG and AXI bus transactions.

Fault injection scenarios are scripted in MATLAB, providing full control over fault location, timing and type. The platform injects SEUs into different locations within the deployed design, including data memory, configuration registers and control logic, where each location produces a distinct effect manifestation at the system level, ranging from Silent Data Corruption (SDC) to Single Event Functional Interrupt (SEFI). This corresponds to the dominant failure mechanisms identified in earlier experiments, where memory-origin upsets propagate through the processing chain to produce SDC or escalate into SEFIs. The BER checker provides real-time link quality measurement during injection campaigns, enabling direct observation of the relationship between injected faults and communication link degradation.

The digital injection pathway directly informs mitigation design. By mapping which functional blocks and fault types produce link-level errors, the platform identifies where techniques such as Triple Modular Redundancy (TMR), Error Correcting Code (ECC) and configuration scrubbing should be applied. Mitigation effectiveness can then be verified by repeating the same campaigns on the mitigated design, closing the rapid learning cycle within the laboratory environment.

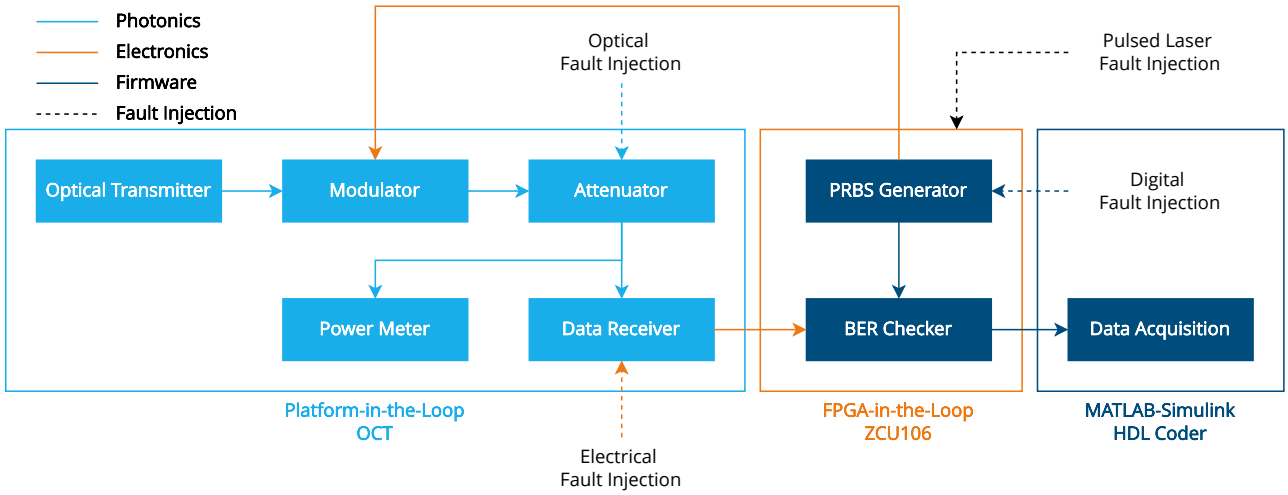


Fig. 2: Architecture of the multi-pathway HiL fault injection platform. The platform provides four injection pathways: digital fault injection through the Simulink/Hardware Description Language (HDL) Coder interface into the FPGA fabric, electrical fault injection through pulse generator-driven transients on component I/Os, optical fault injection through a fibre-coupled noise source into the receiver path, and pulsed laser fault injection targeting the detector and FPGA.

C. Electrical Fault Injection

Electrical fault injection targets the analogue interfaces between components on the PCB, emulating SETs as they would appear at component I/O pins. A pulse generator produces transient voltage signals with controlled amplitude, width and timing, injected directly onto signal lines at component boundaries. This approach reproduces the propagation of SETs through analogue signal chains using pulse-driven transients rather than particle irradiation [9]. A primary use case of this pathway is the study of SET propagation behaviour, including the evolution of individual transients through analogue stages, their progression through cascaded components, and their cross-domain conversion into digital upsets at downstream interfaces. Key observables include transient pulse attenuation and broadening through the signal chain, upset thresholds at downstream digital interfaces, and the effectiveness of filtering or guarding measures at component boundaries.

D. Optical Fault Injection

An unused fibre port in the receiver path provides a direct injection point for optical noise injection. A fibre-coupled light source introduces controlled optical disturbances into the receiver chain, emulating the signal degradation mechanisms that produce the power-independent BER floor identified in previous experiments. The choice of optical noise injection as the laboratory analogue of the radiation-induced BER floor is motivated by preliminary observations that the dominant degradation mechanism, increased optical noise at the receiver input, can be reproduced through controlled fibre-coupled noise injection without the need for particle irradiation. Optical fault injection operates at the signal level within the fibre-coupled path, disturbing the data stream as experienced by the receiver under radiation-degraded link conditions, rather than at the device level where the disturbance would be generated or detected.

Injection amplitude, duration and timing are precisely controlled and synchronised with the data stream. Key observables include receiver BER, Automatic Gain Control (AGC) recovery time, clock recovery loop stability and Forward Error Correction (FEC) decoder performance. By varying injection parameters, the platform maps the receiver fault tolerance envelope, informing decisions on design margins, FEC code selection and link budget reserves.

E. Pulsed Laser Fault Injection

Pulsed laser testing targets the semiconductor material of the photonic receiver and the FPGA, reproducing the charge generation mechanisms of particle-induced SETs at the device level. A focused laser pulse deposits energy in the active region of the semiconductor, generating photocurrents analogous to those produced by ionising particle strikes [10], [18]. This technique is increasingly recognised as complementary to particle beam testing for SEE investigations, enabling device-level characterisation of SET susceptibility without beam facility access. Pulsed laser fault injection occupies an intermediate position between fully in-house laboratory injection and particle beam testing. Specialised laser equipment or access to a partner facility is still required, but the entry threshold and scheduling constraints are substantially lower than for particle beam facilities, making the technique a practical bridge between laboratory iteration and beam validation.

F. Combined Fault Campaigns

The injection pathways can be operated simultaneously to evaluate system-level fault propagation under combined fault

scenarios. A SEU injected into the clock recovery logic via the HDL Coder interface can be combined with an optical disturbance or electrical transient to assess whether the system tolerates concurrent faults across domains. These combined scenarios are representative of in-flight conditions, where parametric degradation in the photonic domain and stochastic upsets in the electronic domain act on the system simultaneously rather than in isolation. A representative use case is the evaluation of FEC effectiveness against radiation-induced bit errors. Controlled optical transient injection emulates the power-independent BER floor while the digital pathway monitors decoder performance, providing a laboratory-accessible pathway to assess coding gain before committing to beam facility qualification. The combined approach also supports evaluation of cross-domain fault propagation, providing insight into system-level failure modes difficult to characterise through single-domain testing alone.

G. Platform Status

The hardware platform is assembled and undergoing commissioning. The ZCU106 evaluation board is operational and interfaced with MATLAB via the Simulink/HDL Coder toolchain, with basic read and write access to the FPGA fabric confirmed. The PRBS generator and BER checker are being implemented in the FPGA fabric. The optical bench includes fibre-coupled laser sources and monitoring equipment, with the communication link path under alignment and characterisation. Initial fault injection experiments will focus on SEU emulation in processing registers, progressing to Multi-Bit Upset (MBU) scenarios and combined multi-pathway campaigns.

IV. Discussion

The progressive RHA methodology and multi-pathway HiL fault injection platform address a practical gap in qualifying COTS-based SmallSat avionics for missions beyond LEO. The asymmetry between photonic and electronic failure modes summarised in Table I is the central observation motivating the multi-pathway architecture. Photonic subsystems exhibit predominantly parametric degradation bounded through end-of-life margin allocation in the link budget. Electronic subsystems, particularly FPGA-based digital processing, are susceptible to discrete, stochastic failure modes directly threatening system availability and requiring active mitigation such as ECC, scrubbing and redundancy. The multi-pathway architecture integrates digital, electrical, optical and pulsed laser injection within a single platform, enabling combined campaigns that capture cross-domain fault propagation, which single-domain approaches cannot.

The progressive approach offers tangible schedule, risk mitigation and cost advantages over traditional qualification schemes. In a conventional workflow, radiation qualification occurs late in the development cycle, after design decisions have been made and hardware has been built. Discovering a vulnerability at this stage forces costly redesign or acceptance of residual risk under schedule pressure. The progressive methodology allows for earlier risk identification. Laboratory-based fault injection surfaces design-relevant vulnerabilities while the architecture is still open to revision, and beam facility time, the most constrained and expensive resource in the RHA process, is reserved for targeted validation of the specific devices and mechanisms identified as critical by the inner loop. This front-loading of knowledge reduces the likelihood of late-stage surprises and enables more efficient allocation of qualification budgets, an important consideration for resource-constrained SmallSat programmes.

While the methodology is presented here on photonic and electronic OCT avionics, the three-stage structure, the use of laboratory-based fault injection as the inner-loop iterating activity, and the use of radiation testing both for design validation and for refining the predicted effects are designed to generalise to other COTS-based avionics facing radiation exposure. The multi-pathway concept extends naturally to mixed-domain systems sharing a similar architectural structure, including COTS FPGA-based payload processors with sensitive analogue front-ends such as mixed-signal radio frequency chains. The platform architecture, built around commercially available evaluation boards and standard toolchains, is reproducible without specialised infrastructure.

V. Conclusion

This paper has presented a progressive, feedback-driven RHA methodology for COTS-based SmallSat avionics targeting orbits beyond LEO. The methodology nests a fast inner loop of laboratory fault injection between system design and mitigation choices inside a slower outer loop in which radiation testing validates the design and refines the predicted effects driving subsequent iterations. The asymmetry between photonic parametric degradation and electronic stochastic failure modes directly motivated the multi-pathway HiL fault injection platform architecture, integrating digital, electrical, optical and pulsed laser injection within a single laboratory environment.

Several open questions remain for the commissioning phase. The fidelity of optical noise injection and pulsed laser fault injection relative to actual radiation-induced transients in the receiver chain requires quantitative validation, particularly whether laboratory-injected disturbances reproduce the temporal profile and amplitude distribution of particle-induced effects. For the electrical pathway, the correspondence between pulse generator-driven transients on component I/Os and radiation-induced SETs observed under irradiation will determine how accurately laboratory campaigns can represent orbital fault environments. For the digital pathway, the relationship between SEU injection density achievable through the Simulink/HDL Coder interface and the fault rates observed under particle irradiation requires similar calibration. Further investigation into the role of FEC in mitigating the power-independent BER floor is enabled by the platform, with implications for link budget design and coding overhead trade-offs.

Results from these activities will inform the outer feedback loop and the targeted validation campaigns it supports. The methodology and platform architecture offer a practical, scalable path towards radiation assurance for SmallSat missions operating beyond LEO.

REFERENCES

[1] J. Budroweit and H. Patscheider, "Risk assessment for the use of COTS devices in space systems under consideration of radiation effects," *Electronics*, vol. 10, no. 9, p. 1008, Apr. 2021.

[2] M. J. Campola and J. A. Pellish, "Radiation hardness assurance: Evolving for NewSpace," RADECS Short Course, 2019.

[3] J. Dijks, S. de Jong, A. Menicucci, and I. Akay, "Systematic review of engineering and testing approaches for radiation hardness assurance in commercial space avionics," *Acta Astronautica*, vol. 238, pp. 1354–1366, 2026.

[4] B. Forlin, E. S. Cishugi, M. Sheikh, T. T. Smit, K.-H. Chen, N. Alachiotis, and M. Ottavi, "Designing dependable systems through a test-in-the-loop method," ser. SEFUW: SpacE FPGA Users Workshop, 6th Edition, 2025.

[5] B. Forlin, K. Böhmer, C. Cazzaniga, P. Rech, G. Furano, N. Alachiotis, and M. Ottavi, "From ground to orbit: A robust and efficient test methodology for risc-v soft-cores," *IEEE Transactions on Device and Materials Reliability*, vol. 25, no. 1, pp. 27–36, 2025.

[6] A. Coronetti, R. García Alía, J. Budroweit, T. Rajkowski, I. Da Costa Lopes, K. Niskanen, D. Söderström, C. Cazzaniga, R. Ferraro, S. Danzeca, J. Mekki, F. Manni, D. Dangla, C. Virmontois, N. Kerboub, A. Koelpin, F. Saigné, P. Wang, V. Pouget, A. Touboul, A. Javanainen, H. Kettunen, and R. C. Germanicus, "Radiation hardness assurance through system-level testing: Risk acceptance, facility requirements, test methodology, and data exploitation," *IEEE Transactions on Nuclear Science*, vol. 68, no. 5, pp. 958–969, May 2021.

[7] M. Moradi, B. Van Acker, K. Vanherpen, and J. Denil, "Model-implemented hybrid fault injection for Simulink (tool demonstrations)," in *Cyber Physical Systems. Model-Based Design (CyPhy/WESE 2018)*, ser. Lecture Notes in Computer Science, vol. 11615. Springer, Cham, 2019, pp. 71–90.

[8] O. Ruano, F. García-Herrero, L. A. Aranda, A. Sánchez-Macián, L. Rodriguez, and J. A. Maestro, "Fault injection emulation for systems in FPGAs: Tools, techniques and methodology, a tutorial," *Sensors*, vol. 21, no. 4, p. 1392, 2021.

[9] V. Ferlet-Cavrois, V. Pouget, D. McMorrow, J. R. Schwank, N. Fel, F. Essely, R. S. Flores, P. Paillet, M. Gaillardin, D. Kobayashi, J. S. Melinger, O. Duhamel, P. E. Dodd, and M. R. Shaneyfelt, "Investigation of the propagation induced pulse broadening (pipb) effect on single event transients in soi and bulk inverter chains," *IEEE Transactions on Nuclear Science*, vol. 55, no. 6, pp. 2842–2853, 2008.

[10] S. P. Buchner, F. Miller, V. Pouget, and D. P. McMorrow, "Pulsed-laser testing for single-event effects investigations," *IEEE Transactions on Nuclear Science*, vol. 60, no. 3, pp. 1852–1875, 2013.

[11] G. Terrasanta, M. Ziarko, N. Bergamasco, M. Poot, and J. Poliak, "Photonic integrated circuits for optical satellite links: A review of the technology status and space effects," *International Journal of Satellite Communications and Networking*, 2025.

[12] M. Hosseinzadeh, J. W. Teng, D. Nergui, B. L. Ringel, A. Ildefonso, A. Khachatrian, D. McMorrow, and J. D. Cressler, "Analysis of optical single-event transients in integrated silicon photonics Mach–Zehnder modulators for space-based optical communications," *IEEE Transactions on Nuclear Science*, vol. 71, no. 4, pp. 736–743, 2024.

[13] Royal Belgian Institute for Space Aeronomy (BIRA-IASB), "SPENVIS: Space environment information system," 2025. [Online]. Available: http://spenvis.oma.be

[14] S. Agostinelli *et al.*, "Geant4—a simulation toolkit," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 506, no. 3, pp. 250–303, 2003.

[15] J. Dijks, S. de Jong, A. Menicucci, I. Akay, and N. Donkers, "Comparative investigation of radiation-driven failure mechanisms in photonic–electronic optical communication terminals across Earth orbits," *IEEE Access*, 2026, submitted.

[16] J. Dijks, S. de Jong, A. Menicucci, I. Akay, and G. Rauwerda, "Workload-dependent radiation response of fault-tolerant RISC-V soft-cores on a PolarFire FPGA under proton irradiation," *IEEE Transactions on Nuclear Science*, 2026, submitted.

[17] L. M. A. Caseiro, D. Caires, and A. M. S. Mendes, "Prototyping power electronics systems with Zynq-based boards using Matlab/Simulink — a complete methodology," *Electronics*, vol. 11, no. 7, p. 1130, 2022.

[18] L. P. Andrus, J. H. Warner, W. C. Rice, A. C. Le, and C. B. Saltonstall, "A rapid, pulsed laser testing approach for single event latchup screening," *IEEE Transactions on Nuclear Science*, 2025.