Low SWaP Flight Board for High-Speed On-Board Data Handling, Processing and AI Inference

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***Abstract* — The continuous increase in payload data volume and mission autonomy requirements is driving the need for increasingly advanced on-board data handling and processing technologies in satellite systems. Next-generation Earth observation, telecommunications, and distributed space architectures require high-performance processing capabilities to enable real-time data reduction, intelligent decision-making, and efficient use of downlink resources.**

In the framework of an ESA-funded project, the High-Performance Computing Edge Extension (HPCEX) high-performance flight board for on-board data handling and processing has been developed to address these challenges. The proposed architecture is based on a dual-FPGA design, enabling parallel high-throughput data processing and robust system management within a single flight-qualified module. The board supports advanced on-board data processing functions and Artificial Intelligence (AI) algorithms through a GPU-like accelerator implemented on FPGA: GPU@SAT IP Core. It executes Machine Learning and Computer Vision workloads directly in orbit without the need for dedicated CPU or external controllers.

As the next step, the development of an additional flight board based on a high-performance processor is going on, targeting high-performance computing (HPC) and satellite communications (SATCOM) applications. The combination of FPGA-based processing, AI acceleration, and high-performance processors will enable the creation of UNIQ, a complete and versatile on-board computing unit, capable of addressing the demanding requirements of future space missions.

The modular architecture has been designed to maximize flexibility and scalability, supporting different mission profiles and processing demands. In parallel, UNIQube, a miniaturized PC/104-compliant version of UNIQ, is currently under development, specifically targeting small satellite platforms with stringent constraints in terms of size, weight, and power. This evolution aims to extend high-performance on-board processing capabilities to small satellite missions without compromising performance or reliability.

The presented work highlights the scalable and forward-looking approach followed by IngeniArs S.r.l. to provide a solution for on-board processing, enabling intelligent, high-throughput satellite systems for both current and future space applications.

Keywords—Flight Unit, On-Board Data Processing, Payload Computer, Instrument Control Unit, Smart Mass Memory Unit, Artificial Intelligence, Satellites Communications, FPGA

I. INTRODUCTION

In recent years, the increasing complexity of space missions has driven a substantial growth in on-board computational requirements. Emerging applications, including high-resolution Earth observation, autonomous navigation, payload data reduction, adaptive telecommunications, and Artificial Intelligence (AI)-based inference [1][2][3], require processing capabilities that significantly exceed those traditionally provided by space-qualified avionics. At the same time, such functionalities must be implemented under stringent constraints in terms of reliability, radiation tolerance, size, weight, and power consumption. Nevertheless, the availability of space-grade processing platforms capable of simultaneously providing high performance, flexibility, modularity, and scalability across different mission classes remains limited [4][5].

This technological gap becomes even more evident when considering the broad spectrum of target applications, ranging from high-end institutional missions to New Space Economy (NSE) and cost-sensitive platforms, each characterized by distinct constraints and operational requirements. Consequently, future on-board computing architectures must not only deliver substantial computational capability, but also support heterogeneous workloads, enable reconfigurability, and adapt to multiple mission profiles without requiring fully custom hardware developments [5][6].

To address these challenges, IngeniArs developed HPCEX, a high-performance flight board designed for on-board data handling and processing. The proposed solution is based on a dual-FPGA architecture integrating a Microchip RTG4 radiation-tolerant FPGA [9] and an AMD Kintex UltraScale KU060 FPGA [10] within a single flight-capable unit. This architecture allows the consolidation of robust system control and management functions together with high-throughput payload data processing, thereby providing a flexible and scalable platform for advanced space applications. In addition, HPCEX enables the execution of AI-based algorithms directly on board through the integration of GPU@SAT [7][8], an FPGA-based GPU-like accelerator IP Core specifically developed to support Machine Learning and Computer Vision workloads without the need for dedicated CPUs or external controllers. A first prototype has been already developed and tested, proving the AI-based processing capabilities, while the development and qualification of the HPCEX Engineering Qualification Model (EQM) is still ongoing.

As a further evolution of this concept, the development of a complete flight computing unit, referred to as UNIQ, is also currently underway. In this architecture, HPCEX is complemented by a HPSC Module (HPSCM), a second processing board based on the Microchip PIC64-HPSC processor [11] and AMD Zynq UltraScale+ RFSoC technology [12], with the additional integration of a Mass Memory Unit. The combination of these heterogeneous computing elements results in a versatile and powerful platform capable of supporting both software-intensive and programmable-logic-intensive applications. Finally, a third flight board is integrated, to receive the external unregulated

power, handle it and distribute the regulated supply to HPSCM and HPCEX boards, guaranteeing EVOPRO to be a self-standing solution also in terms of power management.

Such architecture is intended to address demanding use cases, including High-Performance Computing (HPC), SATCOM, and mass memory management, while preserving the robustness and reliability required for space deployment. The resulting UNIQ unit is conceived as a complete, flexible, and modular solution for advanced on-board processing, perfect as Payload Computer or Instrument Control Unit (ICU). By combining high-performance programmable devices with radiation-tolerant and radiation-hardened components, UNIQ is designed to provide both very high computational performance and the level of resilience required for reliable operation in harsh radiation environments.

Engineering Models (EMs) of both HPSCM and Power Board are actually under development and will be connected to the HPCEX prototype to create the UNIQ EM.

The UNIQ flight unit primarily targets institutional missions, including Class-1 and Class-2 missions, in a 6U Eurocard form factor. In parallel to UNIQ development, a miniaturized PC/104-compliant version, called UNIQube, is being designed to address missions characterized by more stringent mechanical, power, and cost constraints, particularly in the context of small satellite platforms. This compact solution will adopt a more cost-effective approach based on Commercial Off-The-Shelf (COTS) components, while preserving the key architectural principles of modularity, processing capability, and flexibility. The objective is to extend advanced on-board computing functionalities to a broader class of missions, including resource-constrained platforms that nevertheless require increasingly sophisticated on-board data processing capabilities.

This work presents the architectural rationale underlying these developments and outlines a scalable approach to next-generation on-board computing. By combining FPGA and SW-based computing, AI-oriented processing, modular design, and heterogeneous resources, the proposed solutions aim to provide an effective response to the evolving requirements of both current and future space missions.

The paper is organized as follows:

- Section II describes the starting point of the project, i.e., the HPCEX processing board, designed for on-board AI-based data processing, and presenting the development status.
- Section III provides a description of UNIQ, the complete flight solution, deployable for several purposes like payload computing and instrument control unit, born as extension of HPCEX
- Section IV presents UNIQube, the miniaturized version of UNIQ, designed to respond to the strict mechanical and cost requirements of New Space Economy market and cost-sensitive missions.
- Section V draws the conclusions.

II. Flight Board for On-Board Data Processing: HPCEX

Under an INCUBED project [13], supervised by European Space Agency (ESA), the HPCEX board has been conceived as a space-qualified processing platform for high-performance on-board computing, specifically addressing applications requiring parallel data processing and the execution of Artificial Intelligence (AI) algorithms. The board is designed to provide a flexible and scalable hardware architecture, capable of supporting demanding payload data handling functions while ensuring the robustness and reliability required for space deployment.

A key design objective of HPCEX is adaptability across different mission and integration scenarios. The architecture allows a significant degree of customization, including the possibility of supporting High-Speed Serial Links (HSSLs) other than SpaceFibre [14], as well as accommodating mission-specific interface arrangements in which control signals and telemetry may be provided through the front panel rather than through the backplane.

From an architectural standpoint, HPCEX is centered on a heterogeneous dual-device approach, as shown in Figure 1.

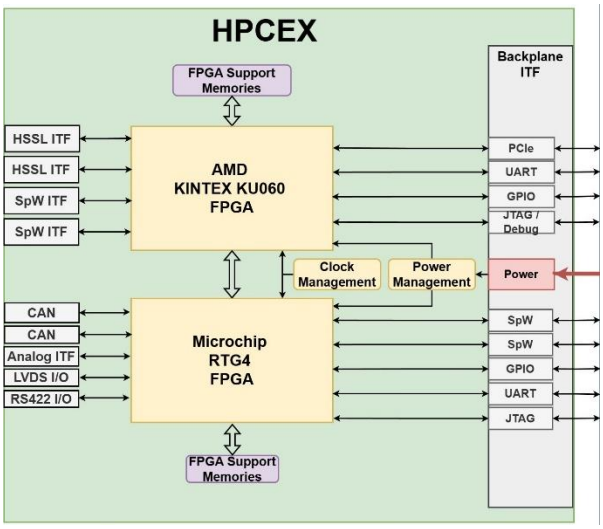

Figure 1 HPCEX high-level architecture

The main processing resource is a high-end space-qualified FPGA based on the AMD Kintex UltraScale+ KU060, which acts as the primary computational element of the board. This device implements high-speed interfaces for scientific data handling and provides the hardware resources required for advanced parallel processing. In addition, it hosts the GPU@SAT IP core, enabling the acceleration of AI-oriented workloads such as Machine Learning and Computer Vision directly on board.

The main FPGA is complemented by a radiation-hardened companion FPGA based on the Microchip RTG4, which operates as the board system controller. This device is responsible for a set of critical and highly reliable functions, including the programming of the AMD KU060 and the scrubbing of its CRAM block, as well as Fault Detection, Isolation and Recovery (FDIR), radiation mitigation, and telemetry/telecommand (TM/TC) management. This architectural partitioning separates high-performance processing from board supervision and critical control, thereby improving the overall robustness of the system. The companion FPGA is included in the EM/EQM versions of the

HPCEX board, whereas the reduced-EM configuration includes only the main FPGA.

The board also integrates the supporting subsystems required for autonomous and reliable operation. These include a power management system for both FPGAs, with dedicated power sequencing functionality, and a clock generation circuitry providing both the input clocks for the programmable devices and the low-jitter reference clocks required for the GTH transceivers of the KU060 FPGA. In addition, the board includes an on-board ADC for the acquisition of external ASM/TSM signals, thus extending the telemetry and monitoring capabilities of the platform.

To sustain high-throughput processing and configuration management, HPCEX also integrates several memory resources. In particular, the main FPGA is supported by an external DDR4 memory, while a dedicated Flash memory is provided for storage of the FPGA bitstream. These memory elements enable both runtime data buffering and non-volatile configuration storage, which are essential for complex processing chains and flexible board operation.

From the connectivity perspective, HPCEX provides a set of front-panel interfaces intended for payload integration and spacecraft interaction. These include two SpaceWire interfaces [15], two HSSL interfaces, and two CAN bus interfaces. In addition, the board supports digital discrete input/output interfaces compatible with single-ended, LVDS, and RS422 electrical standards, allowing the management of discrete signals such as PPS or discrete telemetry lines. The front panel also includes analog input channels for external telemetry acquisition. Besides mission-oriented interfaces, the board provides several additional services and debug interfaces. Through the back panel, the platform exposes dedicated JTAG interfaces for both the main and companion FPGA, as well as UART buses and additional debug I/O pins. These resources support board configuration, validation, low-level monitoring, and integration activities during development and test phases. Finally, HPCEX is designed to operate in conjunction with a custom backplane, exploiting PCIe communication through SpaceVPX connectors. This solution enables high-speed interconnection with companion boards and facilitates integration within more complex modular flight architectures, such as the UNIQ processing unit described in the following section.

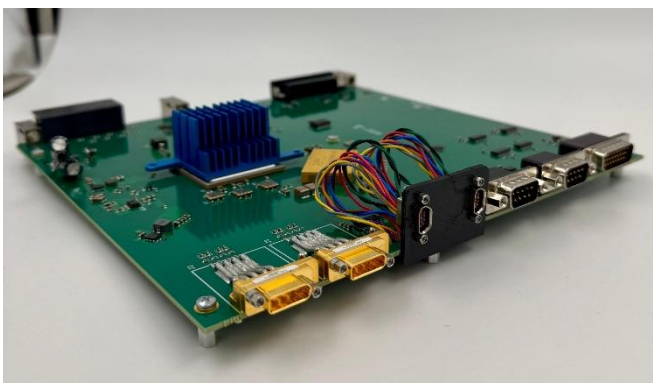

Figure 2 HPCEX Flight Board – Prototype

The ESA activity will result in an EQM, including qualification tests to prove its capability to work in the harsh space environment. A first prototype of HPCEX board has been already developed and manufactured and is depicted in Figure 2.

The prototype has already undergone functional testing, successfully demonstrating the AI-processing capabilities of GPU@SAT IP Core implemented in the programmable logic of the AMD Kintex UltraScale+ KU060. A first test case was carried out by implementing an edge detection algorithm on GPU@SAT, using as input several images provided through high-speed interfaces to emulate the acquisition chain of a scientific imaging payload. This application is representative of an on-board data processing task, for instance cloud detection in Earth observation missions. More specifically, the algorithm processes three input images, representative of RGB channels, each with a resolution of 798 × 798 pixels, and executes three kernels, one for each input image. Figure 3 shows one of the input images used, with the produced output. The implementation of the algorithms has been completed in 555ms, proving a very good performance for an on-board processing.

Figure 3 Input (left) and output (right) images of edge detection algorithm run on HPCEX prototype

A second test case was executed on GPU@SAT using a more complex computer-vision algorithm representative of a typical satellite navigation application. The algorithm processes an image acquired by an onboard camera and provides the optical observables required by the navigation function, namely the estimated range to the Moon and the projection of the Moon centroid onto the image plane. The processing chain, includes an initial coarse edge-detection stage based on the Sun direction, followed by an edge-refinement step exploiting a Laplacian-of-Gaussian filter. The extracted edges are then corrected to sub-pixel accuracy through the use of Zernike moments, while outliers are rejected by means of the RANSAC algorithm. Finally, the Christian-Robinson method is applied to estimate the Moon radius and image centroid [16][17].

This test case is significantly more demanding than the previous one, as it is representative of a 243-layer deep network. The algorithm was successfully executed with a total computation time of 182 s and the quantization-induced error remained limited, with a mean absolute error of 961.3 on the range estimate, 2.90 pixels on the x-centroid estimate, and 1.25 pixels on the y-centroid estimate. In normalized output terms, this corresponds to 1.42%, 0.45%, and 0.26%, respectively. These results confirm the suitability of the

proposed architecture even for the execution of advanced vision-based navigation algorithms and demonstrate compatibility with the performance requirements typically associated with this class of applications.

The design and manufacturing of HPCEX EQM is currently ongoing. In this version, components much closer to the final flight configuration, including higher-reliability and radiation-robust parts will be used to support environmental qualification and demonstrate the suitability of the design for subsequent Proto-Flight Model (PFM) PFM and Flight Model (FM) developments. A comprehensive qualification campaign will then be performed on the EQM, including vibration (sinusoidal and random profiles) and thermal vacuum testing. The EQM is expected to be fully validated by Q3 2026. The EQM will therefore demonstrate the maturity and soundness of the proposed architecture, paving the way for the development of a PFM and, subsequently, a Flight Model FM, by reusing the same architectural approach and replacing the current devices with fully space-grade components.

III. HPCEX EXTENSION: UNIQ

The UNIQ flight unit has been conceived as extension of HPCEX module, to create a modular and space-qualified on-board processing platform addressing advanced data handling, high-performance computing, satellite communications, and mass memory management within a single integrated architecture. The unit is designed to support a broad spectrum of mission scenarios by combining high-performance programmable logic, reliable software-oriented processing, dedicated communication resources, and robust power management. From a functional standpoint, UNIQ architecture is intended to provide five major capabilities:

i) High-performance computing for advanced data processing, parallel computation, and execution of Artificial Intelligence (AI) algorithms
ii) Highly reliable software-based processing for high-performance computer functions and payload data handling
iii) Satellite communications through Intermediate Frequency (IF) radio-frequency interfaces for both Payload Data Transmission (PDT) and Telemetry, Telecommand and Control (TT&C)
iv) Non-volatile mass memory for secure storage of scientific and mission data
v) Autonomous power control and distribution for the regulation and delivery of the electrical power required by all internal subsystems

A key design objective of UNIQ is architectural flexibility. The extensive adoption of programmable devices, including FPGAs and high-performance processors, enables the system to be configured according to mission-specific requirements, thus supporting a wide range of applications and payload classes. This flexibility is complemented by the availability of standardized interfaces, which ensure interoperability with multiple sub-units and external payloads. In particular, the unit supports interfaces such as SpaceFibre, WizardLink, Ethernet TSN, SpaceWire, CAN bus, LVDS, and GPIO, thereby facilitating integration in heterogeneous spacecraft architectures.

A. System-Level Architecture

As shown in Figure 4, the UNIQ unit is organized around three space-qualified Printed Circuit Boards (PCBs) and a dedicated backplane. These elements together define four main architectural building blocks. The first layer is HPCEX, deeply described in section II. The second layer is HPSCM, a space-qualified board combining a high-performance processor, a programmable logic device, and a non-volatile memory subsystem. This layer is responsible for software-based processing, implementation of reliable and safety-critical functions, management of communication tasks, and storage of scientific data through an integrated Mass Memory Unit. The third layer is the Power Board, which performs power conversion, regulation, and distribution. This board receives the external input supply and provides the voltage rails required by the HPCEX and HPSCM boards, thereby ensuring correct operation of the complete flight unit.

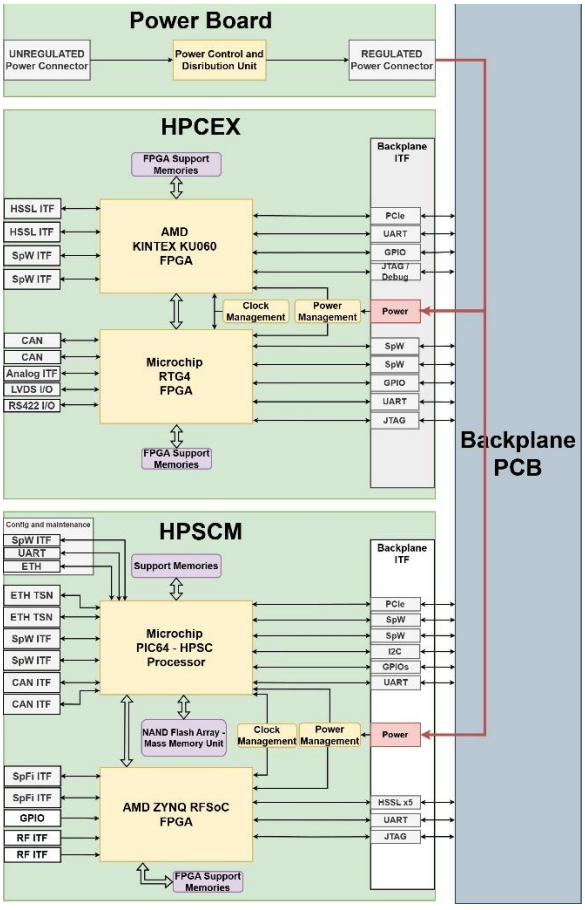

Figure 4 UNIQ high-level architecture

These three boards are interconnected through a dedicated backplane PCB, implemented using SpaceVPX connectors. The backplane performs a central role in the system by distributing regulated power, supporting high-speed data transfer, and managing low-level control interconnections between the processing subsystems. In particular, it provides the regulated power interfaces from the Power Board to the processing boards, high-speed PCIe links between HPCEX

and HPSCM for scientific data exchange before and after AI-based processing, and GPIO-based interconnections between the Microchip RTG4 FPGA on HPCEX and the Microchip PIC64-HPSC processor on HPSCM for status monitoring and telemetry/telecommand exchange.

B. Main Processing Modules and Interfaces

The main capabilities of UNIQ are implemented through a set of heterogeneous processing, memory, power, and interconnection elements, each addressing a specific functional domain within the flight unit. The architecture of HPCEX board has been already presented in section II. The HPSCM board complements this architecture through a combination of software-oriented processing, programmable logic, and non-volatile storage. Its core element is the Microchip PIC64-HPSC processor, which provides high computational performance through eight 64-bit RISC-V cores, support for 512-bit vector operations, and clock frequency up to 1 GHz. At the same time, it offers advanced dependability features, including WorldGuard hardware partitioning and dual-core lockstep mode, making it suitable for reliable execution of safety-critical applications, payload data handling, and integrated Smart PDHU functions. The board further includes an AMD Zynq UltraScale+ RFSoC, which supports both TT&C and Payload Data Transmission (PDT) through IF RF interfaces and integrated ADCs/DACs, while also contributing additional programmable logic resources. Scientific and mission data storage is provided by an integrated Mass Memory Unit, with configurable reliability levels ranging from commercial to radiation-tolerant and radiation-hardened solutions.

Power conversion and regulation are performed by the dedicated Power Board, which receives the external power supply and generates the voltage rails required by the other subsystems.

The three main boards are interconnected through a backplane PCB based on SpaceVPX connectors [18], which distributes regulated power and routes both data and control signals. In particular, the backplane implements high-speed PCIe links between HPCEX and HPSCM for scientific data exchange, together with GPIO interconnections for status monitoring and telemetry/telecommand transfer between the main control elements. The UNIQ flight unit provides a rich set of external interfaces to support integration with payloads, spacecraft subsystems, and ground communication chains. On the front panel, the unit exposes scientific data interfaces including four SpaceWire, four HSSL, and two Ethernet TSN links. Telemetry and telecommand connectivity is provided through four CAN bus interfaces, digital discrete I/O supporting single-ended, LVDS, and RS422 standards, and analog input channels for external telemetry acquisition. The front panel also includes two IF RF interfaces and the external power supply input. Additional interfaces for configuration, maintenance, and debugging are also available, including SpaceWire, UART, and Ethernet service links, as well as JTAG, I2C, and UART buses accessible from the back panel.

C. Typical Operational Scenario

A representative operational scenario for UNIQ foresees the unit acting as a central element in the spacecraft data chain, interfacing with one or more payloads and performing the roles of Payload Computer, Instrument Control Unit, and Smart Mass Memory Unit. In this configuration, shown in Figure 5, UNIQ receives scientific data generated by the payloads, manages command and telemetry exchange with the platform, performs on-board processing, stores mission data, and supports downlink toward ground.

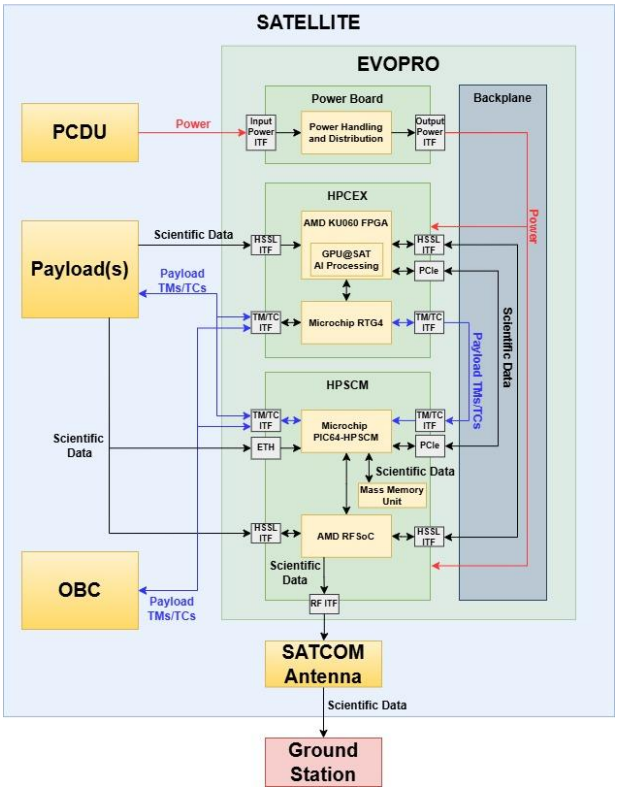

Figure 5 UNIQ operational scenario

In a typical mission profile, raw payload data are acquired through high-bandwidth links and routed to the internal processing resources of the unit. Owing to its flexible and modular architecture, UNIQ can allocate the reception and first-stage handling of such data according to the specific mission configuration, operational constraints, or redundancy strategy. This enables the system to adapt to different payload layouts while preserving consistent system-level behavior. Once acquired, the scientific data can be processed on board according to the mission objectives. In particular, UNIQ enables advanced processing functions aimed at extracting relevant information directly in orbit, thus reducing the amount of raw data to be transmitted to ground and improving the overall efficiency of the mission data chain. From a system perspective, this allows the unit to support near-real-time data exploitation and to implement intelligent processing strategies in which only selected, compressed, or enhanced information is retained for subsequent transmission. In parallel with scientific data processing, UNIQ also manages the control path between spacecraft platforms and payloads. The unit receives telecommands from the spacecraft avionics, dispatches them to the appropriate instruments, and collects

housekeeping and status telemetry from the payload side. This function ensures continuous coordination between the platform and hosted instruments, allowing payload operations and data processing activities to proceed in a coherent and reliable manner. A further key aspect of the operational scenario concerns data storage and transmission. Depending on the mission concept, UNIQ can store raw data, processed data, or both, thereby supporting different strategies for buffering, prioritization, and data retention. The same unit also interfaces with the communication subsystem to support the transfer of payload data toward ground. In this way, acquisition, processing, storage, and downlink are integrated into a single coordinated architecture, enabling an efficient end-to-end data flow from payload generation to final transmission.

This operational scenario is representative of the UNIQ capability to act as a multifunctional and flexible on-board computing unit, capable of integrating payload control, data management, intelligent processing, and communication support within a single system-level architecture.

D. Development Status

The development of the UNIQ flight unit is currently progressing through an incremental and modular approach. A first HPCEX prototype has already been developed and is being used to validate the key high-performance and AI-processing functionalities of the system. In parallel, the Engineering Models (EMs) of the Power Board and of the HPSCM module are currently under design. The integration of these three board-level EMs will enable the realization of the first UNIQ unit-level EM, which will be used to validate communication among the boards and, more generally, to assess the end-to-end processing capabilities of the complete system. The UNIQ EM is expected to be ready by Q4 2026. According to the current roadmap, the next development step after the EM phase will be the realization of the EQMs of the two remaining modules, in addition to HPCEX, in order to achieve a complete UNIQ EQM at unit level. This qualification model will be used to perform the relevant environmental test campaign and to demonstrate the suitability of the architecture for subsequent Proto-Flight Model (PFM) and Flight Model (FM) developments.

IV. PC-104 FLIGHT UNIT: UNIQUBE

As a further evolution of the UNIQ concept, UNIQube is being developed as a miniaturized version of the flight unit specifically targeting small satellite platforms and cost-sensitive missions. The main objective of UNIQube is to preserve the functional capabilities of UNIQ while addressing the more stringent constraints typically associated with this class of missions, in particular in terms of size, integration complexity, and cost. To this end, UNIQube adopts a PC-104 form factor, with a modular architecture, leveraging commercial components wherever compatible with the target mission requirements. As demonstrator of the final low Size, Weight and Power (SWaP) processing unit, the mechanical housing of UNIQube has been already designed and produced, and it is shown in Figure 6.

Figure 6 UNIQube flight unit

The electronic boards of UNIQube are under development, derived from the same architectural principles of UNIQ, but following the main paradigm to distribute UNIQ main functionalities across six specialized layers, resulting in a highly flexible and scalable solution. This approach would enable mission-dependent tailoring of the overall system configuration, while maintaining support for advanced on-board processing, control, communication, memory management, and power distribution.

The main functional blocks of the HPCEX processing board are planned to be distributed over the first two layers. The first layer will be based on the AMD Kintex UltraScale+ KU060 FPGA, which will provide the high-performance programmable logic resources required for intensive data processing, parallel computation, and AI-oriented workloads. This layer will represent the main acceleration engine of the architecture. The second layer will host the controller module, which will be dedicated to the supervision and control of the AMD Kintex UltraScale+ KU060 FPGA. This function will be implemented either through a Microchip RTG4 FPGA or through a radiation-hardened processor, depending on the target configuration and mission requirements. In both cases, the purpose of this layer will be to ensure reliable control of the main processing FPGA and to support critical management functions.

Similarly, the main functional blocks of HPSCM are intended to be distributed over three additional PCBs. The third layer of UNIQube will implement the software-processing capability through the integration of the Microchip PIC64-HPSC processor. This module will be intended to execute reliable software-based applications, including platform control functions and payload data handling tasks, thus complementing the FPGA-based high-performance processing domain. Satellite communication capabilities will be provided by the fourth PCB, based on the AMD RFSoC device. This module will enable the implementation of communication functions through programmable logic and integrated RF resources, thereby supporting advanced SATCOM applications within the modular architecture. Mass data storage will be assigned to the fifth layer, which will implement an array of NAND Flash memory devices. This

module will provide the non-volatile storage capability required for payload and mission data, while allowing the memory capacity and technology selection to be adapted to specific mission constraints. Finally, the last PCB will perform the management, conversion, and distribution of electrical power to all the other modules, thereby ensuring proper powering conditions for the complete unit.

Overall, UNIQube is being developed as an extension of the same architectural approach toward a compact and cost-effective solution for small satellites. By preserving the key functionalities of the original unit and redistributing them over a modular multilayer architecture, UNIQube will provide a flexible platform capable of supporting advanced on-board processing functions even in missions characterized by reduced volume, mass, and budget availability.

V. CONCLUSIONS

This work has presented a scalable and heterogeneous approach to next-generation on-board computing for space applications, addressing the growing demand for high computational performance, flexibility, and robustness across different mission classes. Starting from the HPCEX board, a high-performance space-qualified processing platform based on a dual-FPGA architecture, the proposed development path has evolved toward the definition of UNIQ, a complete flight unit integrating high-throughput programmable processing, reliable software-based computation, satellite communication capabilities, mass memory resources, and power management within a single modular architecture.

The proposed solution combines the advantages of high-performance programmable logic with the reliability of radiation-tolerant and radiation-hardened devices, thus enabling the execution of demanding on-board processing tasks in harsh space environments. In particular, the integration of the GPU@SAT accelerator within the FPGA-based processing chain extends the architecture toward advanced Artificial Intelligence, Machine Learning, and Computer Vision applications, allowing complex workloads to be executed directly on board. At the same time, the introduction of additional heterogeneous computing elements, such as the PIC64-HPSC processor and the RFSoC-based SATCOM layer, broadens the application domain of the system to include high-performance computing, telecommunications, and intelligent payload data handling.

To further extend these capabilities toward smaller and more cost-constrained platforms, the UNIQube architecture has also been introduced as a miniaturized and modular evolution of UNIQ. By redistributing the main functions of the flight unit across multiple specialized layers and leveraging commercial components where appropriate, UNIQube preserves the core functional principles of the original architecture while improving adaptability to small satellite and low-cost mission scenarios.

The presented architecture demonstrates how modularity, heterogeneous processing, and scalable integration can be effectively combined to address both current and future needs in spaceborne computing. The proposed technological roadmap therefore enables a family of processing solutions spanning from high-end institutional missions to cost-sensitive small satellite applications, while maintaining a common architectural vision centered on performance, flexibility, and reliability.

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